**Amendments to the Specification:**

Please replace the paragraph beginning at page 1, line 4, with the following amended paragraph:

This is a continuation-in-part of Application No. 10/106,812, filed March 26, 2002, now U.S. Patent No. 6,903,412, which is a continuation-in-part of Application No. 09/927,143, filed August 10, 2001, now U.S. Patent No. 6,849,898. This is also a continuation-in-part of Application No. 10/326,311, filed December 19, 2002, which is a continuation-in-part of the following applications: Application No. 10/317,568, filed December 12, 2002, now U.S. Patent No. 6,764,906, which is a continuation-in-part of Application No. 09/898,652, filed July 3, 2001, now U.S. Patent No. 6,569,738; Application No. 10/176,570, filed June 21, 2002, now U.S. Patent No. 6,709,930; and Application No. 10/106,812, filed March 26, 2002, which is a continuation-in-part of Application No. 09/927,143, filed August 10, 2001, now U.S. Patent No. 6,849,898. Each of the foregoing applications is incorporated herein by reference in its entirety.

Please replace the paragraph beginning at page 1, line 14, with the following amended paragraph:

This application is related to Application No. 09/927,320, filed August 10, 2001, now U.S. Patent No. 6,882,000, and to Application No. 09/591,179, filed June 8, 2000, each of which is incorporated herein by reference in its entirety.

Please replace the paragraph beginning at page 16, line 28, with the following amended paragraph:

As shown in **Figs. 13A** and **13B**, active regions 500 contain a lattice of trenches 19 which define square MOSFET cells. Source metal layer 17 overlies active regions 500 and makes contact with the source and body regions in each of the cells, as shown in **Fig. 4**, for example. A series of parallel gate fingers 510, which are essentially extensions of trenches 19, extend from active regions 500 to locations below gate bus 504, which is in an inactive region. **Fig. 13C** is a cross-sectional view taken at section 13C-13C in **Fig.**

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**13B**, showing how electrical contact is made between gate bus 504 and the polysilicon gate material within one of gate fingers 510 through an opening in a BPSG (borophosphosilicate glass) layer 512 ~~512,~~. The area of contact between gate bus 504 and the polysilicon gate material is designated 514 in **Figs. 13A-13C**. Gate fingers 510 become slightly wider under gate bus 504 to allow a larger contact area 514. It should be noted that the method of contacting the polysilicon gate material shown in **Fig. 13C** is illustrative and not limiting. As those of skill in the art will know, there are alternative ways of making contact between the gate bus and the gate electrode.

Please replace the paragraph beginning at page 17, line 18, with the following amended paragraph:

The embodiment shown in **Figs. 15A-15B** is somewhat similar to the embodiment shown in **Figs. 14A-14C**, except that gate fingers 520 are more widely spaced than gate fingers 510 and transverse gate finger 522 has wider segments 524 between the intersections with gate fingers 520 ~~510~~. The contacts 526 between gate bus 504 and the polysilicon in gate finger 522 are made in the wider segments 524. This increases the area available for making the contacts while avoiding the problems that may occur in filling the trenches at the intersections between gate fingers 520 and 522 if gate finger 522 is wider than gate fingers 520 (as in embodiment shown in **Figs. 14A-14C**).

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